REMARKS/ARGUMENTS

Claims 1, 6, 26, 29, 30, 32, 34, 35, 38, 39, and 49-53 are pending. Claims 1, 6, 26, 29, 30, 32, 35, 38, and 39 are amended. Claims 49-53 are new. The Specification and drawings are amended. No new matter has been added by any of the amendments or new claims. Reconsideration of the application is respectfully requested.

I. Examiner Interview

The Applicant-initiated Examiner interview of April 1, 2009 included participants Primary Examiner Tuan A. Vu, Inventor Frank Levine, and Applicant's representative A.M. Thompson. The discussion during the interview focused on the objection to the specification, rejections under 35 U.S.C. §101, 35 U.S.C. §112 first and second paragraphs, and the rejection under 35 U.S.C. §103 over *Gover*. Inventor Frank Levine pointed out that the objection rejections applied in the Office Action were valid pursuant to a typographical error in the Specification and the drawings that had only been brought to his attention recently, more specifically, since the Office Action mailed December 18, 2008. Specifically, the typographical error involved the labeling of an instruction cache processing unit as "instruction cache" and the labeling of a data cache processing unit as a "data cache". Mr. Levine concurred with Primary Examiner Vu that the scope of operations and functionality of data cache and an instruction cache is quite limited in comparison to an instruction cache unit and a data cache unit.

Mr. Levine and Applicant's representative pointed out that an instruction cache, as labeled, would not functionally perform all the processing it is disclosed as performing in the disclosure, as originally filed. Accordingly, numerous processing examples were highlighted in the interview which supported the correction of a scrivener's error wherein all instances of "instruction cache" and "data cache" are amended to recite "instruction cache unit" and "data cache unit", respectively.

Mr. Levine and Applicant's representative insisted that this change did not constitute new matter as there was no change in the function of the elements despite the name change. Functionally, the erroneously labeled elements performed the same. The only difference involved semantics, *i.e.* ***instruction cache unit*** and ***data cache unit*** instead of instruction cache and data cache. The change of terminology is required at least to achieve consistency in the

specification and drawings which feature a plurality of units, and to achieve a clarification of the invention and remove the confusion based on the incorrect element labels which resulted in the misapplied objections and rejections.

The courtesies extended to the inventor and Applicant's representative during the interview is sincerely appreciated, especially here, where the lengthy and complicated agenda consumed an inordinate amount of the time of Primary Examiner Tuan Vu. The suggestions and consideration offered by Primary Examiner Tuan Vu provided tremendous insight into the unfortunate inconsistencies present in the application as originally filed, and has been invaluable in making the amendments required to restore the accuracy of the application.

II. Double Patenting Rejection

The Office Action provisionally rejects claims 1, 6 and 34 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over various claims of copending Applications including Application 10/675,777, Application 10/675,778, Application 10/675,872, Application 10/682,385 and Application 10/675,721.

The filing of any Terminal Disclaimers to obviate the obviousness-type double patenting rejections will occur subsequent to a determination of allowable subject matter being indicated in the claims.

III. Objections to the Specification

The Office Action objects to the Specification because it includes terminology which is different from that which is generally accepted in the art. Specifically, the Office Action states that the terms "instruction cache" and "data cache" are functionally inconsistent with the performance of these elements in the computer fields. The Office Action states in pertinent part:

> (i) "Instruction cache 300 processes instructions for execution ... instruction cache 300 determines which instructions are associated with indicators . . . when instruction cache 300 determines that an instruction . . .is present" (Specifications: 1st para, 2nd para, pg 23). The actions termed as 'processes' and 'determines' (as underlined) used in a context where *instruction cache* 300 is actually performing *processing* and *determining* is not a well-accepted terminology in the closest and related computer fields of using *instruction cache*.

Office Action of December 18, 2008, page 7, paragraph 8, Section (i).

The Office Action further states:

> (iii) 'the data and indicators are processed by a data cache, such as data cache 216 . . . data cache sends signals indicating that marked memory locations' (last para pg. 24). One familiar with the art of using or implementing cache cannot accept functionality of cache in terms being able to process data and actively transmit signals, absent clear teaching provided by the Disclosure to that regard.

Office Action of December 18, 2008, page 8, Section (iii).

The Office Action required a clarification of instruction cache and data cache and states:

> Applicant is required to provide a clarification of these matters or correlation with art-accepted terminology so that a proper comparison with the prior art can be made. Applicant should be careful not to introduce any **new matter** into the disclosure (i.e., matter which is not supported by the disclosure as originally filed).

Office Action of December 18, 2008, page 8, Section (iii), last paragraph.

Applicant has provided clarification of the terminology that triggered the objections to the Specification. Specifically, each instance of "instruction cache" and "data cache" in the drawings and disclosure, as originally filed, are amended to state "instruction cache unit" and "data cache unit", respectively. This amendment is consistent with the described functionality of these elements in the disclosure. These amendments obviate the objections to the specification. Accordingly, it is respectfully requested that these amendments be entered and the objections to the specification be withdrawn.

IV. 35 U.S.C. § 101

The Office Action rejects claims 1, 6, 26, 29, 30, 32, 34, 35, 38, and 39 under 35 U.S.C. § 101 because the claimed invention is not supported by a specific and substantial asserted utility or a well established utility. This rejection of the claims, as amended, is respectfully traversed.

The claims and the specification are amended to conform to the functionality described in the disclosure, as originally filed. The Office Action states in pertinent part:

> The language regarding how the instruction cache operates … amounts to a far-fetched terminology without evidence of utility (e.g. specific and established programmatic or hardware means in place) to corroborate to the credibility of such terminology and feasibility of how the instruction cache can provide and achieve the operation of determining, processing or sending.

Office Action of December 18, 2008, paragraph 10.

During the Applicant initiated interview, inventor Mr. Levine clarified that the instruction cache and the data cache provided the functionality of an instruction cache ***unit*** and the data cache ***unit***, and accordingly should have been so denoted in the drawings and the disclosure as originally filed. Therefore, the claims and the drawings of the disclosure are now amended in accordance with the functionality expressed in the disclosure, as originally filed. The amendments obviate the rejection of claims 1, 6, 26, 29, 30, 32, 34, 35, 38 and 39 under 35 U.S.C. §101. Accordingly, it is therefore respectfully requested that this rejection be withdrawn.

V. 35 U.S.C. § 112, First Paragraph

The Office Action rejects claims 1, 6, 26, 29, 30, 32, 34, 35, 38, and 39 under 35 U.S.C. § 112, first paragraph stating that the claimed invention is not supported by either a specific and substantial asserted utility or a well established utility. The rejection of the claims, as amended, is respectfully traversed.

The Office Action states in pertinent part:

> According to the analysis of the Specifications and the observations made in the §101 rejection, the instruction cache is nowhere taught by the Disclosure as equipped with programmatic or hardware functionality in terms of executed actions *of processing, determining* then *sending.*

Office Action of December 18, 2008, page 11, paragraph 12.

In the Applicant-initiated interview of April 1, 2009, inventor Frank Levine indicated that instances of "instruction cache" in the disclosure, as originally filed, should have been denoted as "instruction cache **unit**" consistent with the functionality of processing, determining and sending outlined in the disclosure. Accordingly, the disclosure and the claims are now amended to correct this oversight/ scrivener's error. The amendment to include the term "unit" clarifies the utility of the instruction cache unit which, as originally disclosed, contains additional logic that supports the actions of processing, determining, and sending and therefore provides support for the use of the term. The rejection of the claims under this code section is therefore obviated. Accordingly, it is respectfully requested that the rejections be withdrawn.

VI. 35 U.S.C. § 112, Second Paragraph

The Office Action rejects claims 32, 36, *sic*, 38, and 39 under 35 U.S.C. § 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of

elements, such omission amounting to a gap between the necessary structural connections. The rejection of these claims, as amended, is respectfully traversed.

Here again, the Office Action becomes mired in confusion over the seemingly broad scope and meaning of the term "instruction cache". The Office Action states in pertinent part:

> [t]There is an omission of essential teaching. One cannot construe a external code for determining and sending by the cache when the code for such resides in the computer readable medium that has nothing in common with the recited 'instruction cache'. The lack of functionality of the cache (in terms of established utility) and the lack of relationship between determining and sending by cache and determining and sending by the computer medium code would not enable one to make use of the invention.

Office Action of December 18, 2008, page 13, paragraph 3.

During the Applicant initiated Examiner interview of April 1, 2009, inventor Mr. Levine clarified that instances of "instruction cache" in the disclosure, as originally filed, should have been denoted as "instruction cache **unit**" consistent with the functions provided by this element in the disclosure as originally filed. The claims in the disclosure amend all instances of "instruction cache" to instruction cache unit, consistent with the functionality already described in the disclosure. Further, all instances of "data cache" are amended to **data cache unit**, consistent with the described functionality of this feature in the disclosure, as originally filed. The amendments obviate the rejection of the claims under this code section. Accordingly, it is respectfully requested that the rejections be withdrawn.

VII. 35 U.S.C. § 103

The Office Action rejects claims 1, 6, 26, 29, 30, 32, 34, 35, 38, and 39 under 35 U.S.C. § 103(a) as being obvious over *Gover et al.* ("*Gover*"), U.S. Patent 5,752,062, in view of admitted prior art. The rejection of the claims, as amended, is respectfully traversed.

35 U.S.C. § 103 requires a highly fact-dependent analysis involving taking the claimed subject matter as a whole, and comparing it to the prior art. *KSR Int'l. Co. v. Teleflex, Inc.*, 550 U.S. 398, 82 USPQ2d 1385(2007). Further, "[a]ll words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Claim 1 is representative and recites:

> 1. A computer implemented method in an instruction cache of a data processing system for monitoring execution of instructions, the method comprising:
>
> receiving a bundle at an instruction cache unit, the bundle containing at least one instruction slot, wherein the instruction slot contains an instruction;
>
> responsive to receiving the bundle, determining by the instruction cache unit whether the bundle contains an indicator within at least one spare bit of the at least one instruction slot, wherein the indicator identifies the instruction as one that is to be monitored by a performance monitor unit;
>
> responsive to a determination that the bundle contains the indicator within the at least one instruction slot, sending a signal by the instruction cache unit to a performance monitor unit, wherein upon receiving the signal, the performance monitor unit increments a counter in the instruction cache unit that is associated with the instruction, the incrementing providing a count of a number of times the instruction is executed; and
>
> sending the bundle from the instruction cache unit to a functional unit for execution of the instruction.

The claims require the feature of an ***instruction cache unit***. This feature represents a fundamental distinction between the claims and the cited art of *Gover*. *Gover* discloses an instruction cache that functions in accordance with instruction caches well know to one skilled in the art. Specifically, the instruction cache of *Gover* stores instructions. *Gover* discloses in pertinent part:

> If one or more of the sequence of instructions is not stored in instruction cache 14. then instruction cache 14 inputs (through BIU 12 and system bus 11) such instructions from system memory 39 connected to system bus 11. In response to the instructions input from instruction cache 14. sequencer unit 18 selectively dispatches through a dispatch unit 46 the instructions to selected ones of execution units....

Gover, column 5, lines 24-34.

Additional traditional uses of the instruction cache are disclosed throughout *Gover*. For example, *Gover* further discloses:

> In the fetch stage. sequencer unit 18 **selectively inputs (from instructions cache 14) one or more instructions** from one or more memory addresses storing the sequence of 10 instructions discussed further hereinabove in connection with branch unit 20 and sequencer unit 18. the decode stage. sequencer unit 18 decodes up to four fetched instructions.

Gover, column 6, lines 7-12 (emphasis added).

By contrast, the claims feature an ***instruction cache unit*** that includes additional logic for processing data, *e.g.* counting, selecting, and transmitting data. One representation of the disclosed instruction cache unit recited in the claim is illustrated in Figure 31, reproduced *infra*.

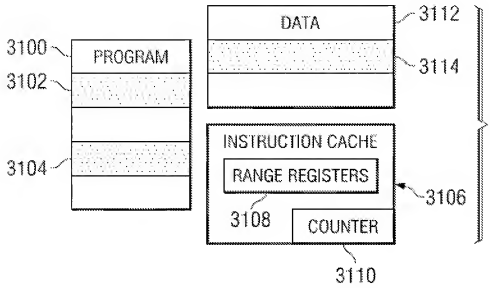

FIG. 31

In FIG. 31, instance 3106 of illustrates an instruction cache unit that includes a counter space 3110, and range registers 3108 that may function in conjunction with counter 3110. Accordingly, it must be noted that the instruction cache unit possessed components that enable a processing capability which exceeds the functionality of the common **instruction cache** disclosed in *Glover*. For at least this reason along, the cited art of Glover cannot read on the claims. The asserted Admitted prior art, *i.e.* pages 2-3 of the specification, adds nothing to cure the deficiencies in *Glover*. Nowhere in the background of the disclosure is there any reference to an **instruction cache unit** that performs processing as disclosed in the claims.

In summary, *Glover* and the asserted admitted prior art do not collectively or individually teach or fairly suggest an ***instruction cache unit***. Therefore, for at least this reason a conclusion of *prima facie* obviousness cannot be established. It is well-settled that to establish a prima facie case of obviousness, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981,985, 180 USPQ 580 (CCPA 1974).

Accordingly, it is respectfully requested that the rejection of claims 1, 6, 26, 29, 30, 32, 34, 35, 38 and 39 as obvious over *Glover* in view of Admitted Prior Art be withdrawn.

VIII. New Claims

Claims 49-53 are newly added to further recite the allowable subject matter of the disclosure. Support for the claims may be found in the specification as originally filed, and more specifically at FIG. 3, FIG. 4, FIG. 8, pages 23, 24, 30, 31, 35 and 36. No new matter is added. The new claims include the feature of an instruction cache unit which as indicated, *supra*, distinguishes over the cited art of *Glover* and the admitted prior art.

IX. Conclusion

The subject application is patentable over the cited reference of *Gover* and is now in condition for allowance, a notice of which is respectfully requested.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite prosecution or aid the examination of this application.

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Respectfully submitted,

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